CLAIMS

1. A semiconductor memory having a burst mode reading function of continuously reading data in synchronization with a clock signal comprising:

a memory array composed of a plurality of memory cells;

a sync read control circuit for releasing an upper group of a received address as a memory access address in synchronization with the clock signal and for sequentially modifying and releasing as a burst address a remaining of the received address excluding the upper group in synchronization with the clock signal;

a sense amplifier for amplifying a small output signal received from each of the memory cells selectively determined by the memory address and releasing the amplified signal as an output data;

a decoder for decoding the burst address;

a burst latch for latching and releasing the decoded burst address in synchronization with the clock signal; and

a page selector for holding the output data and selecting corresponding one of the output data determined by the burst address.

2. A semiconductor memory having a burst mode reading function of continuously reading data in synchronization with a clock signal comprising:

a memory array composed of a plurality of memory cells;

a sync read control circuit for releasing an upper group of a received address as a memory access address in synchronization with the clock signal

and for sequentially modifying and releasing as a burst address a remaining of the received address excluding the upper group in synchronization with the clock signal;

a sense amplifier for amplifying a small output signal received from each of the memory cells selectively determined by the memory address and releasing the amplified signal as an output data;

a decoder for decoding the burst address;

a burst latch for latching and releasing the decoded burst address in synchronization with the clock signal;

a page selector for holding the output data and selecting corresponding one of the output data determined by the burst address; and

an output latch for latching and releasing the output data selected by the page selector in synchronization with the clock signal.

3. The semiconductor memory according to claims 1 or 2, wherein

the sync read control circuit is arranged to increment the burst address in synchronization with the clock signal starting from a timing of the (N-1)th clock pulse where N being a predetermined number of clock pulses of the clock signal between a release of a burst mode start signal and the output of the output data.

4. A semiconductor memory having a burst mode reading function of continuously reading data in synchronization with a clock signal comprising:

a memory array composed of a plurality of memory cells;

a sync read control circuit for releasing an upper group of a received address as a memory access address in synchronization with the clock signal and for sequentially modifying and releasing as a burst address a remaining of the received address excluding the upper group in synchronization with the clock signal;

a sense amplifier for amplifying a small output signal received from each of the memory cells selectively determined by the memory address and releasing the amplified signal as an output data;

a decoder for decoding the burst address;

a burst latch for latching and releasing the decoded burst address in synchronization with the clock signal;

a page selector for holding the output data and selecting corresponding one of the output data determined by the burst address; and

an output latch for latching and releasing the output data selected by the page selector in synchronization with the clock signal, wherein

the burst latch and the decoder are arranged to develop a composite circuit with the burst latch being a flip-flop comprising a master circuit and a slave circuit, the master circuit connected at an upstream side of the decoder and the slave circuit connected at a downstream side of the decoder.

5. The semiconductor memory according to claim 4, wherein

the sync read control circuit is arranged to increment the burst address in synchronization with the clock signal starting from a timing of the (N-1)th clock pulse where N being a predetermined number of clock pulses of the clock signal between a release of a burst mode start signal and the output

of the output data.

6. The semiconductor memory according to claim 5, wherein

the composite circuit is arranged in which the burst address latched by the master circuit is decoded by the decoder and then latched by the slave circuit.

7. The semiconductor memory according to claim 6, wherein

the composite circuit has an output address switching function for releasing the burst address when it is at a burst read mode and directly releasing a lower address when it is at an asynchronous read mode.

8. An address control circuit provided in a semiconductor memory, wherein

the address control circuit is constructed as a composite circuit having a master circuit of a flip-flop connected at an upstream side of a decoder and a slave circuit of the flip-flop connected at a downstream side of the decoder, which is arranged responsive to a read switching signal, a clock signal, a synchronous address signal synchronized with the clock signal, and an asynchronous address signal received from the outside, and

when the read switching signal is at a synchronous read mode, the composite circuit selects the synchronous address signal, latches the synchronous address signal with the clock signal in the master circuit of the flip-flop, decodes the latched synchronous address signal with the decoder, and latches the decoded synchronous address signal with the clock signal in

the slave circuit of the flip-flop, and alternatively when the read switching signal is at an asynchronous read mode, the flip-flop becomes conductive and the decoder decodes and releases the asynchronous address signal.

9. The address control circuit according to claim 8, wherein

the composite circuit is arranged for decoding the synchronous address signal latched by the master circuit with the decoder and latching the decoded synchronous address signal with the slave circuit.

10. The address control circuit according to claim 9, wherein

the composite circuit has an output address switching function of releasing the synchronous address signal when it is at the synchronous read mode and directly releasing the asynchronous address signal when it is at the asynchronous read mode.